Claims

1. A semiconductor package, comprising:

a substrate in which a plurality of terminals for a test and a plurality of terminals for external connection are arranged over a front surface, a plurality of terminals for internal connection are arranged over a back surface, and an internal connection of the terminal for internal connection is made to the desired terminal for a test and/or the terminal for external connection;

at least one semiconductor chip in which a plurality of surface terminals connected to an internal circuit are formed over a front surface, and which is arranged so that a back surface may face the back surface of the substrate;

a wiring which connects the surface terminal of the semiconductor chip to the desired terminal for internal connection of the substrate; and

a molded member which seals the semiconductor chip over the back surface of the substrate.

2. A semiconductor package according to claim 1, wherein

a predetermined action can be made to the semiconductor chip via the terminal for external connection of the substrate by a desired connection between the surface terminal of the semiconductor chip, and the terminal for internal connection of the substrate, and a desired connection between the terminal for internal connection and the terminal for external connection of the substrate.

3. A semiconductor package according to claim 2, wherein

two or more groups of the terminals for internal connection of the substrate are formed; and

a different action can be made to the semiconductor chip by a first desired connection between the terminal for internal connection of a first

group, and the terminal for external connection, or a second desired connection between the terminal for internal connection of a second group, and the terminal for external connection, and a desired connection between the surface terminal of the semiconductor chip, and the terminal for internal connection of the first group or the second group of the substrate.

4. A semiconductor package according to claim 1, wherein

a predetermined action of the semiconductor chip can be tested via the terminal for a test of the substrate by a desired connection between the surface terminal of the semiconductor chip, and the terminal for internal connection of the substrate, and a desired connection between the terminal for internal connection and the terminal for a test of the substrate.

5. A semiconductor package according to claim 1, wherein

in the substrate, an arrangement area of the terminals for a test and an arrangement area of the terminals for external connection are separated.

6. A semiconductor package according to claim 5, wherein

in the substrate, the arrangement area of the terminal for external connection is arranged at a periphery of the substrate, and the arrangement area of the terminal for a test is arranged at an inner portion except the periphery of the substrate.

7. A semiconductor package according to claim 5, wherein

in the substrate, the arrangement area of the terminal for external connection is arranged at a periphery of facing two sides of the substrate, the arrangement area of the terminal for a test is arranged at a periphery of another facing two sides of the substrate, and a non-terminal area where a terminal is not arranged is formed in a central part of the substrate.

8. A semiconductor package according to claim 5, wherein

in the substrate, the arrangement area of the terminal for external connection is arranged at a periphery of the substrate, the arrangement area of the terminal for a test is arranged at an inner portion which adjoins the periphery of the substrate, and a non-terminal area where a terminal is not arranged is formed in a central part of the substrate.

9. A semiconductor package according to claim 1, wherein

in the substrate, the terminal for internal connection is arranged at a periphery of the substrate.

10. A semiconductor package according to claim 1, wherein

the one or more semiconductor chips are two or more semiconductor chips stacked in layers.

11. A semiconductor package according to claim 1, wherein

a spacer exposed from the molded member is arranged over the front surface of the semiconductor chip.

12. A semiconductor package according to claim 1, wherein

a part of the wiring is exposed over a front surface of the molded member.

13. A semiconductor package according to claim 1, wherein

an adhesive member is adhered to a front surface of the molded member.

14. A semiconductor package according to claim 5, wherein

the molded member is formed over the back surface of the substrate with fixed thickness, and is formed with relatively small thickness in a portion corresponding to the arrangement area of the terminal for external connection of the substrate.

15. A semiconductor package according to claim 7 or 8, wherein

the substrate has a peripheral part extended outside a periphery side part of the molded member, and the terminal for external connection is arranged at the peripheral part of the substrate.

16. A semiconductor package according to claim 5, wherein

the molded member is formed over the back surface of the substrate with fixed thickness, and is formed so that a rim end portion of the substrate may be wrapped in.

17. A semiconductor package according to claim 1, wherein

the terminal for a test, the terminal for external connection and the terminal for internal connection of the substrate, and the surface terminal of the semiconductor chip are pads for wire bonding, and the wiring is a wire for bonding.

18. A semiconductor device, comprising:

a main substrate in which a plurality of main terminals for connection are arranged over a main front surface, a plurality of main terminals for external connection are arranged over a back surface, and an internal connection of the main terminal for connection is made to the desired main terminal for external connection;

at least one main semiconductor chip in which a plurality of surface terminals connected to an internal circuit are formed in a main front surface, and which is arranged so that a back surface may face the front surface of the main substrate;

at least one semiconductor package according to claim 1 arranged so that the molded member may face the front surface of the main semiconductor chip;

wirings which connect the surface terminal of the main

semiconductor chip, and the terminal for external connection of the semiconductor package to the desired main terminal for connection of the main substrate; and

a main molded member which seals the main semiconductor chip and the semiconductor package over the front surface of the main substrate.

19. A semiconductor device according to claim 18, wherein

the at least one semiconductor package is two or more semiconductor packages stacked in layers into a lower berth and an upper berth, and the semiconductor package of the upper berth is laid in a non-terminal area where the terminal for external connection is not arranged of the semiconductor package of the lower berth.